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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,402	10/17/2001	Yoshihiro Satoh	N32040200W	6789

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EXAMINER

RICHARDS, N DREW

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 12/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/981,402

Applicant(s)

SATOH, YOSHIHIRO

Examiner

N. Drew Richards

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AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 18 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 7-24 is/are pending in the application.
- 4a) Of the above claim(s) 7-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 21-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/17/03 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, and 21-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art.

Applicant's admitted prior art, hereafter referred to as "APA", discloses in figures 16-21 a semiconductor device comprising a contact 30 which penetrates an interlayer insulating film 26 and is electrically connected with a diffusion layer (not shown) in the silicon substrate, a gate electrode 16,18 which is formed on the silicon substrate and

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contains a nitride film 20,24 at upper and side portions, and a silicon nitride film 20,24 for preventing carbon diffusion, having a portion sandwiched between the interlayer insulating film 26 and the silicon substrate while traversing a region except a portion for providing the electrical connection between the contact and the diffusion layer, and is formed on the nitride film at the upper and side portions of the gate electrode. Films 20 and 24 are each considered two separate nitride layers laminated on one another where the first layer (the lower portion of 20 and the inside portion of 24) is the nitride film on the gate electrode while the second layer (the upper portion of 20 and the outside portion of 24) is the silicon nitride film for preventing carbon diffusion. The silicon nitride film for preventing carbon diffusion is sandwiched between the interlayer insulating film 26 and the silicon substrate 12 as shown in figure 16 where the interlayer insulating film 26 is formed above the silicon nitride film 20,24 for preventing carbon diffusion and the substrate 12 is formed below the silicon nitride film. Thus, the silicon nitride film is considered sandwiched as claimed.

With regard to claim 2, the insulating film is disclosed on page 3 lines 8 and 9 as including tantalum oxide ( $\text{Ta}_2\text{O}_5$ ) and the device is disclosed as being a dynamic random access memory having a memory cell capacitor film including the tantalum oxide.

With regard to claim 21, APA discloses a contact 30 which penetrates a first interlayer insulating film 26 and is electrically connected with a diffusion layer (not

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shown) in the silicon substrate, a capacitor contact 46 that is interposed between a lower electrode of the memory cell capacitor (not shown) and the contact 30 while penetrating a second interlayer insulating film 32 and a third interlayer insulating film 32, a conductor 33,34 which is formed on the second interlayer insulating film 32 and contains a nitride film 36,40 at upper and side portions, a fourth interlayer insulating film 42 which is formed on the third interlayer insulating film 32, and a silicon nitride film 36,40 for preventing carbon diffusion having a portion sandwiched between the fourth interlayer insulating film 42 and the third interlayer insulating film 32 while traversing a region except a connection portion between the lower electrode and the capacitor contact, and is formed above the nitride film at the upper portion of the conductor. Film 32 is considered a second interlayer insulator (bottom portion) and a third interlayer insulator (top portion) of the same material formed one on top of the other. Films 36 and 40 are each considered two separate nitride layers laminated on one another where the first layer (the lower portion of 36 and the inside portion of 40) is the nitride film on the conductor while the second layer (the upper portion of 36 and the outside portion of 40) is the silicon nitride film for preventing carbon diffusion. The silicon nitride film for preventing carbon diffusion is sandwiched between the fourth interlayer insulating film 42 and the third interlayer insulating film 32 as shown in figure 17 where the fourth interlayer insulating film 42 is formed above the silicon nitride film 36,40 for preventing carbon diffusion and the third interlayer insulating film 32 is formed below the silicon nitride film. Thus, the silicon nitride film is considered sandwiched as claimed.

With regard to claim 22, the insulating film is disclosed on page 3 lines 8 and 9 as including tantalum oxide ( $\text{Ta}_2\text{O}_5$ ) and the device is disclosed as being a dynamic random access memory having a memory cell capacitor film including the tantalum oxide.

With regard to claim 23, APA discloses a contact 30 that is electrically connected with a diffusion layer (not shown) formed in the silicon substrate while penetrating a first interlayer insulating film 26, the contact is electrically connected to a capacitor contact 46 that is interposed between a lower electrode of a memory cell capacitor (not shown) and the contact 30 while penetrating a second interlayer insulating film 32 and a third interlayer insulating film 42 for providing an electrical connection between the lower electrode and the contact, a conductor 33,34 which is formed on the second interlayer insulating film 32 and contains a nitride film 36,40 at upper and side portions, a silicon nitride film 36,40 for preventing carbon diffusion formed between the second and third interlayer insulating films while traversing a region except a connection portion between the lower electrode and the capacitor contact, and is formed on the nitride film at the upper and side portions of the conductor. Films 36 and 40 are each considered two separate nitride layers laminated on one another where the first layer (the lower portion of 36 and the inside portion of 40) is the nitride film on the conductor while the second layer (the upper portion of 36 and the outside portion of 40) is the silicon nitride film for preventing carbon diffusion.

With regard to claim 24, the insulating film is disclosed on page 3 lines 8 and 9 as including tantalum oxide ( $Ta_2O_5$ ) and the device is disclosed as being a dynamic random access memory having a memory cell capacitor film including the tantalum oxide.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Jost et al. (U.S. Patent No. 5,900,660).

Jost et al. disclose in figure 5 a semiconductor device as claimed. Jost et al. disclose :

a contact 36 which penetrates an interlayer insulating film 28 and is electrically connected with a diffusion layer 24 in the silicon substrate 11;

a gate electrode 12,14 which is formed on the silicon substrate 11 and contains a nitride film 18 at upper and side portions;

a silicon nitride film 20 for preventing carbon diffusion, having a portion sandwiched between the interlayer insulating film 28 and the silicon substrate 11 while traversing a region except a portion for providing the electrical connection between the contact 36 and the diffusion layer 24, and is formed on the nitride film 18 at the upper and side portions of the gate electrode.

5. Claims 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura et al. (U.S. Patent No. 5,986,299).

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Nakamura et al. disclose in figure 20 a semiconductor device including an insulating film formed from gas containing carbon comprising:

a contact 110 which penetrates a first interlayer insulating film 108 and is electrically connected with a diffusion layer 103 in the silicon substrate 101;

a capacitor contact 113,116 that is interposed between a lower electrode 119,120 of a memory cell capacitor 120,121,122 and the contact 110 while penetrating a second interlayer insulating film 112 and a third interlayer insulating film 115;

a conductor 114 which is formed on the second interlayer insulating film 112 and contains a nitride film 142 at upper and side portions;

a fourth interlayer insulating film 118 which is formed on the third interlayer insulating film 115;

and a silicon nitride film 143 for preventing carbon diffusion having a portion sandwiched between the fourth interlayer insulating film 118 and the third interlayer insulating film 115 while traversing a region except a connection portion between the lower electrode 119 and the capacitor contact 113,116 and is formed above the nitride film 142 at the upper portion of the conductor.

With regard to claim 22, the insulating film is disclosed as tantalum oxide (column 3 lines 60-62) and the semiconductor device is a dynamic random access memory (DRAM, column 14 line 10) having a memory cell capacitor film including the tantalum oxide.

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6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jost et al. as applied to claim 1 above, and further in view of Applicant's admitted prior art (hereafter "APA").

Jost et al. teaches the semiconductor device is a dynamic access memory having a memory cell capacitor film (DRAM as taught in background section, having capacitor film 38, 40, 42 in figure 5). Jost et al. does not teach the insulating film including tantalum oxide and the tantalum oxide being included in the capacitor. "APA" teach a DRAM using a tantalum oxide film in the capacitor on page 3 lines 8 and 9.

Jost et al. and "APA" are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the tantalum oxide of "APA" in the capacitor of Jost et al. The motivation for doing so is to provide increased capacitance per area taken using the high dielectric constant of the tantalum oxide. Therefore, it would have been obvious to combine Jost et al. with "APA" to obtain the invention of claim 2.

### ***Response to Arguments***

8. Applicant's arguments filed 5/2/03 have been fully considered but they are not persuasive.

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First, with regard to claims 1 and 2, applicant argues that the nitride films 20 and 24 of the APA are single films and that the Examiner's interpretation of nitride films 20 and 24 being two separate films each is erroneous. This is not persuasive as a single silicon nitride film has the same structure as two silicon nitride films formed one on the other as silicon nitride films are amorphous and have no crystals or grain boundaries within the film. Thus, the single nitride film of the APA is structurally equal to the claimed two silicon nitride films and reads on the claims. Applicant supplied evidence that silicon nitride films may be crystalline and not amorphous. However, applicant has not claimed the silicon nitride films being crystalline nor submitted arguments or evidence that the claimed silicon nitride films are crystalline. Applicant's exhibit B shows that silicon nitride films may occasionally be crystalline but does not provide any evidence or reasoning that applicant's silicon nitride film is crystalline.

Second, applicant's arguments with regards to claims 21-24 are not persuasive. Applicant states that their previous arguments with regards to these claims remain unrebutted. The previous arguments were unrebutted because the final rejection of claims 21-24 in Paper No. 14 presented new rejections of claims 21-24. In Paper No. 14 the Examiner made every effort to address those arguments that were relevant to the new rejections. Further, the arguments presented herein combine the rejections of claim 21 and 23 and the interpretations of the APA used in the rejections. The rejections of claims 21 and 23 used two different interpretation of the APA. Thus, it is not clear how the arguments presented herein apply to the final rejection of claims 21

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and 23 separately. Applicant's cited portions (citations 9 and 11-14) are from the previous Office action (Paper No. 12) and thus the arguments rebutting those rejections (from Paper No. 12) are moot in view of the new grounds of rejection (presented in Paper No. 14).

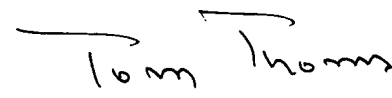
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

  
NDR

  
Tom Thomas  
Supervisor